

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	J1800 MEMORY CONTROLLER
05	J1800 DISPLAY,SATA,SD,GBE
06	J1800 USB,CLK,SPI,LPC
07	J1800 POWER/GND_1
08	J1800 POWER/GND_2
09	DDR3L SO-DIMM CHANNEL A,B
10	SMBUS,SIGNAL L/S
11	PCIE X1 SLOT /MINI PCIE SLOT
12	USB3.0/2.0,CLK BUF
13	HWM,FAN CTRL,-PROCHIT
14	COM,FP,SPK,SATALED,KB/MS
15	ITE 8620 LPC IO
16	SPI SINGLE BIOS
17	Realtek ALC887-VD2
18	REAR AUDIO JACK
19	REALTEK RTL8111F-VL
20	POWER SEQUENCE
21	DISCRETE POWER
22	ATX
23	VCORE ISL95836_1
24	VCORE ISL95836_2,VCORE,VAXG
25	HDMI,LPT
26	GENESYS GL850S

Gigabyte Technology

Title			Cover Sheet
Size	Document Number	GA-J1800N-D2H	Rev
Custom			1.1
Date:	Friday, April 18, 2014	Sheet	1 of 26

Revision 1.1

Component value change history

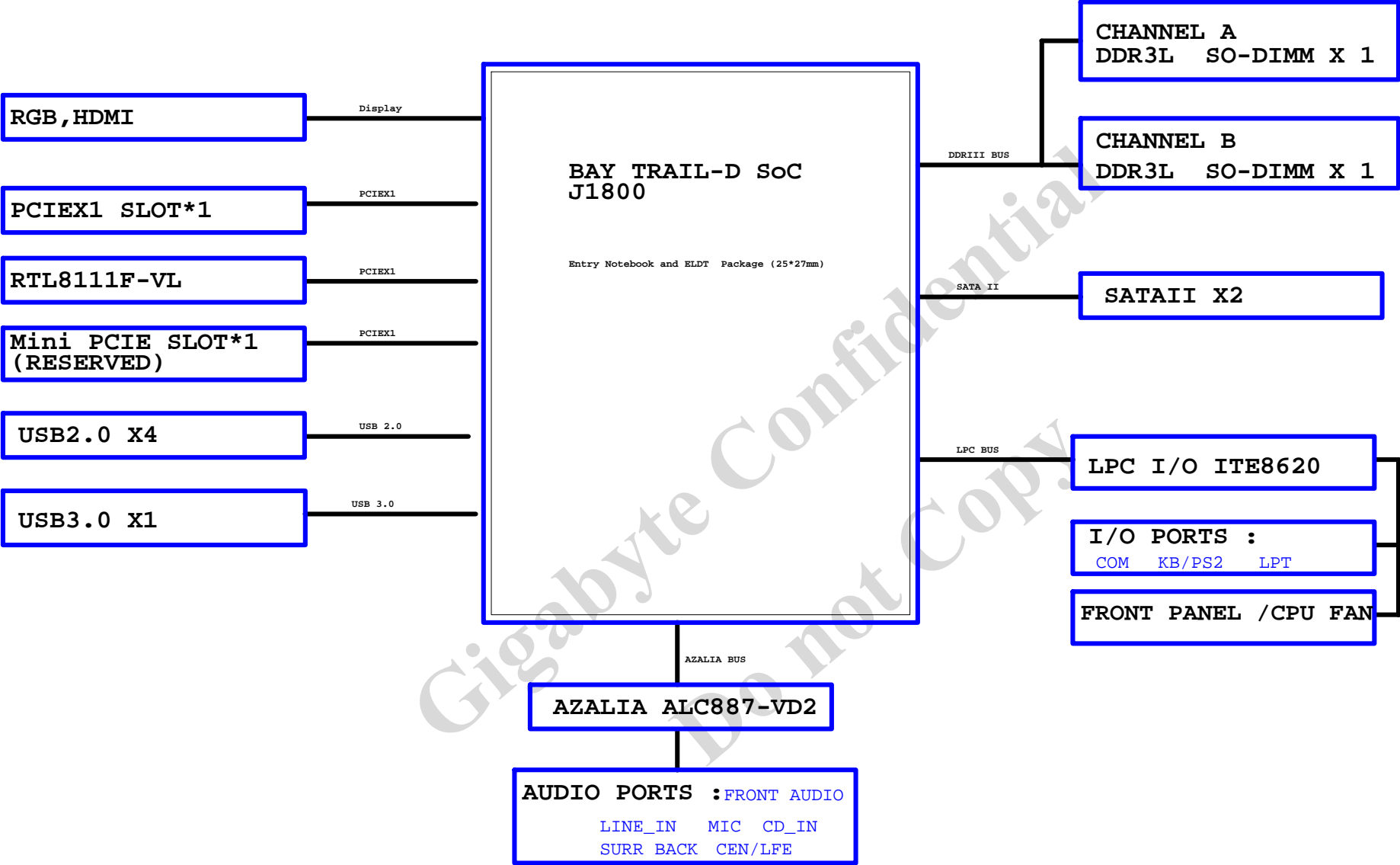
2014/04/18

[illegible]

Circuit or PCB layout change

[illegible]

BLOCK DIAGRAM



DDR0

U1A

MAAA0	K45	DRAM0_MA_0
MAAA1	H47	DRAM0_MA_1
MAAA2	L41	DRAM0_MA_2
MAAA3	H44	DRAM0_MA_3
MAAA4	H50	DRAM0_MA_4
MAAA5	G53	DRAM0_MA_5
MAAA6	H49	DRAM0_MA_6
MAAA7	D50	DRAM0_MA_7
MAAA8	G52	DRAM0_MA_8
MAAA9	E52	DRAM0_MA_9
MAAA10	K48	DRAM0_MA_10
MAAA11	E51	DRAM0_MA_11
MAAA12	F47	DRAM0_MA_12
MAAA13	J51	DRAM0_MA_13
MAAA14	B49	DRAM0_MA_14
MAAA15	B50	DRAM0_MA_15

[9] -SRASA ← -SRASA M45C
[9] -SCASA ← -SCASA M44C
[9] -SWEA ← -SWEA H51C

[9] SBAA0 ← SBAA0 K47
[9] SBAA1 ← SBAA1 K44
[9] SBAA2 ← SBAA2 D52

[9] -CSA0 ← -CSA0 P44C
[9] -CSA2 ← -CSA2 P45C

[9] CKEA0 ← CKEA0 C47
[9] CKEA2 ← CKEA2 X D48
[9] CKEA2 ← CKEA2 F44
[9] CKEA2 ← CKEA2 X E46

[9] MODT_A0 ← MODT_A0 T41
[9] MODT_A2 ← MODT_A2 P42

[9] DCLKA0 ← DCLKA0 M50
[9] -DCLKA0 ← -DCLKA0 M48

[9] DCLKA2 ← DCLKA2 P50
[9] -DCLKA2 ← -DCLKA2 P48

[9] M_DMA0 ← M_DMA0 G36
[9] M_DMA1 ← M_DMA1 B36
[9] M_DMA2 ← M_DMA2 B42
[9] M_DMA3 ← M_DMA3 P51
[9] M_DMA4 ← M_DMA4 V42
[9] M_DMA5 ← M_DMA5 Y50
[9] M_DMA6 ← M_DMA6 Y50
[9] M_DMA7 ← M_DMA7 Y52

[9] -DDR3A_RST ← -DDR3A_RST P41C

DDR3_VREF AF44

DRAM_PWROK AD42
[10] DCORE_PWROK ← DCORE_PWROK AB42

R2 23.2/4/1 DDR3_ODTPU AD44
R3 29.4/4/1 DDR3_DQPU AF45
R4 162/4/1 DDR3_CMDPU AD45

R5 100K/4/1 AF42
R6 100K/4/1 AH42

ICLK_DRAM_TERM
ICLK_DRAM_TERM
RSVD_AF40
RSVD_AF41
RSVD_AD40
RSVD_AD41

J1800/2.41G/C0/SR1UU/[10HB5-621800-20R]

DRAM0_DQ_0	M36	MDA0
DRAM0_DQ_1	J36	MDA1
DRAM0_DQ_2	P40	MDA2
DRAM0_DQ_3	M40	MDA3
DRAM0_DQ_4	P36	MDA4
DRAM0_DQ_5	N36	MDA5
DRAM0_DQ_6	K40	MDA6
DRAM0_DQ_7	K42	MDA7
DRAM0_DQ_8	B32	MDA8
DRAM0_DQ_9	C32	MDA9
DRAM0_DQ_10	C36	MDA10
DRAM0_DQ_11	A37	MDA11
DRAM0_DQ_12	C33	MDA12
DRAM0_DQ_13	A33	MDA13
DRAM0_DQ_14	C37	MDA14
DRAM0_DQ_15	B38	MDA15
DRAM0_DQ_16	F36	MDA16
DRAM0_DQ_17	G38	MDA17
DRAM0_DQ_18	F42	MDA18
DRAM0_DQ_19	J42	MDA19
DRAM0_DQ_20	G40	MDA20
DRAM0_DQ_21	C38	MDA21
DRAM0_DQ_22	G44	MDA22
DRAM0_DQ_23	D42	MDA23
DRAM0_DQ_24	A41	MDA24
DRAM0_DQ_25	C41	MDA25
DRAM0_DQ_26	B46	MDA26
DRAM0_DQ_27	C40	MDA27
DRAM0_DQ_28	B40	MDA28
DRAM0_DQ_29	B48	MDA29
DRAM0_DQ_30	B47	MDA30
DRAM0_DQ_31	K52	MDA32
DRAM0_DQ_32	K51	MDA33
DRAM0_DQ_33	T52	MDA34
DRAM0_DQ_34	T51	MDA35
DRAM0_DQ_35	L51	MDA36
DRAM0_DQ_36	L53	MDA37
DRAM0_DQ_37	R51	MDA38
DRAM0_DQ_38	R53	MDA39
DRAM0_DQ_39	T47	MDA40
DRAM0_DQ_40	T45	MDA41
DRAM0_DQ_41	Y40	MDA42
DRAM0_DQ_42	V41	MDA43
DRAM0_DQ_43	T48	MDA44
DRAM0_DQ_44	T50	MDA45
DRAM0_DQ_45	Y42	MDA46
DRAM0_DQ_46	AB40	MDA47
DRAM0_DQ_47	V45	MDA48
DRAM0_DQ_48	V47	MDA49
DRAM0_DQ_49	AD48	MDA50
DRAM0_DQ_50	AD50	MDA51
DRAM0_DQ_51	V48	MDA52
DRAM0_DQ_52	V50	MDA53
DRAM0_DQ_53	AB44	MDA54
DRAM0_DQ_54	Y45	MDA55
DRAM0_DQ_55	V52	MDA56
DRAM0_DQ_56	W51	MDA57
DRAM0_DQ_57	AC53	MDA58
DRAM0_DQ_58	AC51	MDA59
DRAM0_DQ_59	W53	MDA60
DRAM0_DQ_60	Y51	MDA61
DRAM0_DQ_61	AD52	MDA62
DRAM0_DQ_62	AD51	MDA63
DRAM0_DQ_63		

DRAM0_DQSP_0	J38	DQSA0
DRAM0_DQSP_1	C35	DQSA1
DRAM0_DQSP_2	D40	DQSA2
DRAM0_DQSP_3	B44	DQSA3
DRAM0_DQSP_4	N53	DQSA4
DRAM0_DQSP_5	T42	DQSA5
DRAM0_DQSP_6	Y47	DQSA6
DRAM0_DQSP_7	AB52	DQSA7

DRAM0_DQSN_0	K38	-DQSA0
DRAM0_DQSN_1	B34	-DQSA1
DRAM0_DQSN_2	F40	-DQSA2
DRAM0_DQSN_3	C43	-DQSA3
DRAM0_DQSN_4	M52	-DQSA4
DRAM0_DQSN_5	T44	-DQSA5
DRAM0_DQSN_6	Y48	-DQSA6
DRAM0_DQSN_7	AA51	-DQSA7

DDR1

U1B

MAAB0	AY45	DRAM1_MA_0
MAAB1	BB47	DRAM1_MA_1
MAAB2	AW41	DRAM1_MA_2
MAAB3	BB44	DRAM1_MA_3
MAAB4	BB50	DRAM1_MA_4
MAAB5	BC53	DRAM1_MA_5
MAAB6	BB49	DRAM1_MA_6
MAAB7	BF50	DRAM1_MA_7
MAAB8	BC52	DRAM1_MA_8
MAAB9	BE52	DRAM1_MA_9
MAAB10	AY48	DRAM1_MA_10
MAAB11	BE51	DRAM1_MA_11
MAAB12	BD47	DRAM1_MA_12
MAAB13	BA51	DRAM1_MA_13
MAAB14	BH49	DRAM1_MA_14
MAAB15	BH50	DRAM1_MA_15

[9] -SRASB ← -SRASB AV45C
[9] -SCASB ← -SCASB AV44C
[9] -SWEB ← -SWEB BB51C

[9] SBAB0 ← SBAB0 AY47
[9] SBAB1 ← SBAB1 AY44
[9] SBAB2 ← SBAB2 BF52

[9] -CSB0 ← -CSB0 AT44C
[9] -CSB2 ← -CSB2 AT45C

[9] CKEB0 ← CKEB0 BG47
[9] CKEB2 ← CKEB2 X BE46
[9] CKEB2 ← CKEB2 BD44
[9] CKEB2 ← CKEB2 X BF48

[9] MODT_B0 ← MODT_B0 AP41
[9] MODT_B2 ← MODT_B2 AT42

[9] DCLKB0 ← DCLKB0 AV50
[9] -DCLKB0 ← -DCLKB0 AV48

[9] DCLKB2 ← DCLKB2 AT50
[9] -DCLKB2 ← -DCLKB2 AT48

[9] M_DMB0 ← M_DMB0 BD38
[9] M_DMB1 ← M_DMB1 BH38
[9] M_DMB2 ← M_DMB2 BC36
[9] M_DMB3 ← M_DMB3 BH42
[9] M_DMB4 ← M_DMB4 AT51
[9] M_DMB5 ← M_DMB5 AM42
[9] M_DMB6 ← M_DMB6 AK50
[9] M_DMB7 ← M_DMB7 AK52

[9] -DDR3B_RST ← -DDR3B_RST AT41C

DRAM1_MA_0	BM38	MDB0
DRAM1_MA_1	BC40	MDB1
DRAM1_MA_2	BA42	MDB2
DRAM1_MA_3	BD42	MDB3
DRAM1_MA_4	BC38	MDB4
DRAM1_MA_5	BD36	MDB5
DRAM1_MA_6	BF42	MDB6
DRAM1_MA_7	BC44	MDB7
DRAM1_MA_8	BH32	MDB8
DRAM1_MA_9	BG32	MDB9
DRAM1_MA_10	BG36	MDB10
DRAM1_MA_11	BJ37	MDB11
DRAM1_MA_12	BG33	MDB12
DRAM1_MA_13	BJ33	MDB13
DRAM1_MA_14	BG37	MDB14
DRAM1_MA_15	BH38	MDB15
	AJ36	MDB16
	AT36	MDB17
	AV40	MDB18
	AT40	MDB19
	BA36	MDB20
	AV36	MDB21
	AY42	MDB22
	AY40	MDB23
	BJ41	MDB24
	BG41	MDB25
	BJ45	MDB26
	BH46	MDB27
	BG40	MDB28
	BH40	MDB29
	BH48	MDB30
	BH47	MDB31
	AY52	MDB32
	AY51	MDB33
	AP52	MDB34
	AP51	MDB35
	AW51	MDB36
	AW53	MDB37
	AR51	MDB38
	AR53	MDB39
	AP47	MDB40
	AP45	MDB41
	AK40	MDB42
	AM41	MDB43
	AP48	MDB44
	AP50	MDB45
	AP50	MDB46
	AM40	MDB47
	AH45	MDB48
	AM47	MDB49
	AF48	MDB50
	AF50	MDB51
	AM48	MDB52
	AM50	MDB53
	AH44	MDB54
	AK45	MDB55
	AM52	MDB56
	AL51	MDB57
	AG53	MDB58
	AG51	MDB59
	AL53	MDB60
	AK51	MDB61
	AF52	MDB62
	AF51	MDB63

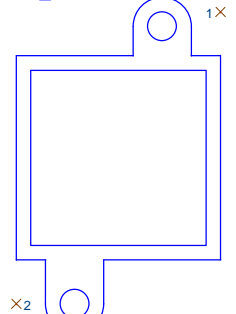
DRAM1_DQSP_0	BF40	DQSB0
DRAM1_DQSP_1	BG35	DQSB1
DRAM1_DQSP_2	BA38	DQSB2
DRAM1_DQSP_3	BH44	DQSB3
DRAM1_DQSP_4	AJ53	DQSB4
DRAM1_DQSP_5	AP42	DQSB5
DRAM1_DQSP_6	AK47	DQSB6
DRAM1_DQSP_7	AH52	DQSB7

DRAM1_DQSN_0	-BD40	-DQSB0
DRAM1_DQSN_1	BH34	-DQSB1
DRAM1_DQSN_2	AY38	-DQSB2
DRAM1_DQSN_3	BG43	-DQSB3
DRAM1_DQSN_4	AY52	-DQSB4
DRAM1_DQSN_5	AP44	-DQSB5
DRAM1_DQSN_6	AK48	-DQSB6
DRAM1_DQSN_7	AJ51	-DQSB7

J1800/2.41G/C0/SR1UU/[10HB5-621800-20R]

HEAT SINK

NB_HEATSINK

FANLESS HEATSINK
COST DOWNSOC_HS
CPU_HS[12SP2-SA0601-01R_12SP2-SA0601-02R_12SP2-SA0601-03R]

[9] MDA[0..63] ↔ MDA[0..63]

[9] MDB[0..63] ↔ MDB[0..63]

[9] DQSA[0..7] ↔ DQSA[0..7]

[9] -DQSA[0..7] ↔ -DQSA[0..7]

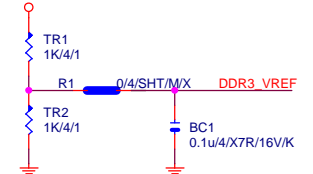
[9] MAAA[0..15] ↔ MAAA[0..15]

[9] MAAB[0..15] ↔ MAAB[0..15]

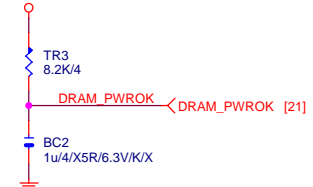
[9] DQSB[0..7] ↔ DQSB[0..7]

[9] -DQSB[0..7] ↔ -DQSB[0..7]

+VCCDDRXXS3_1P35



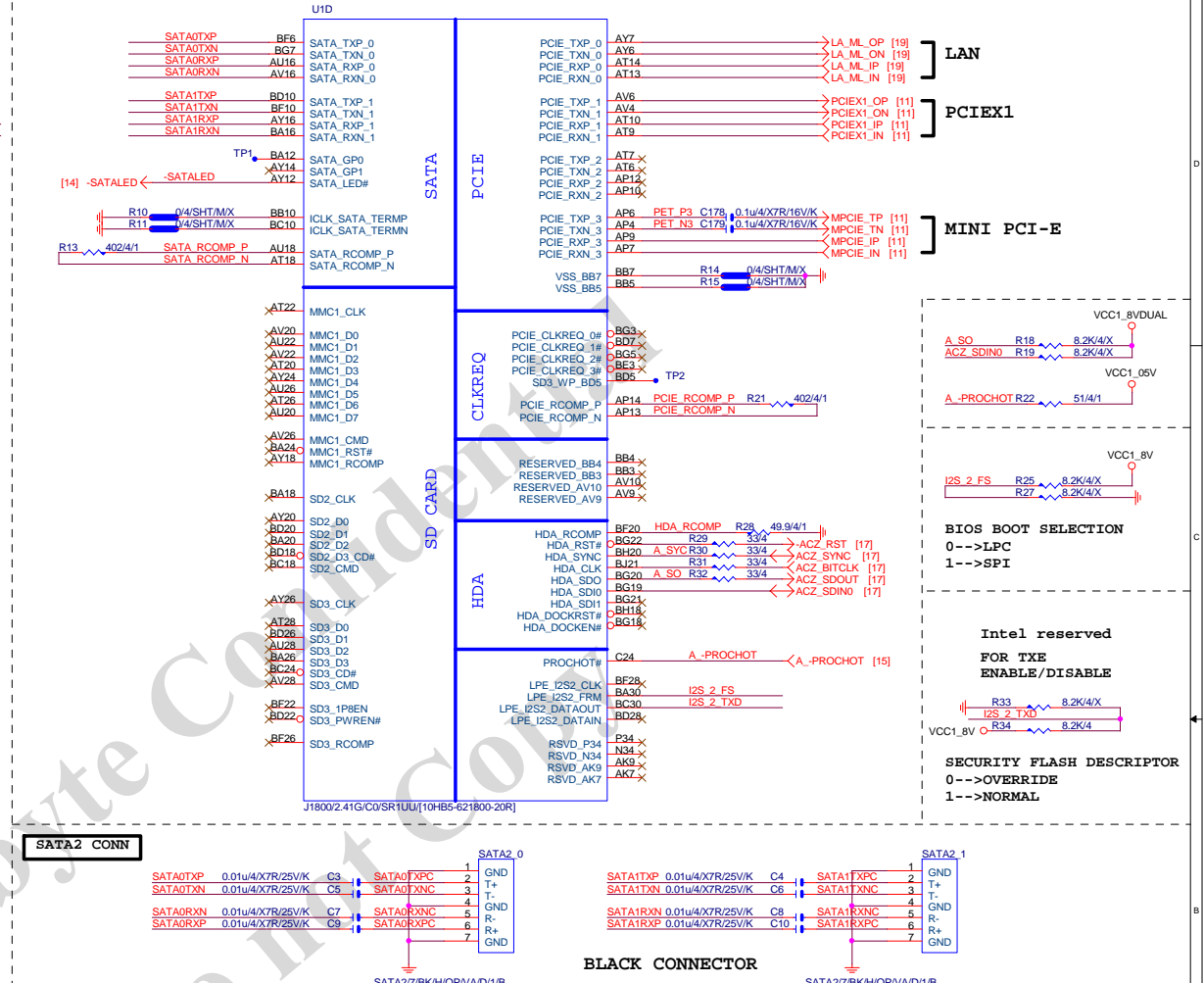
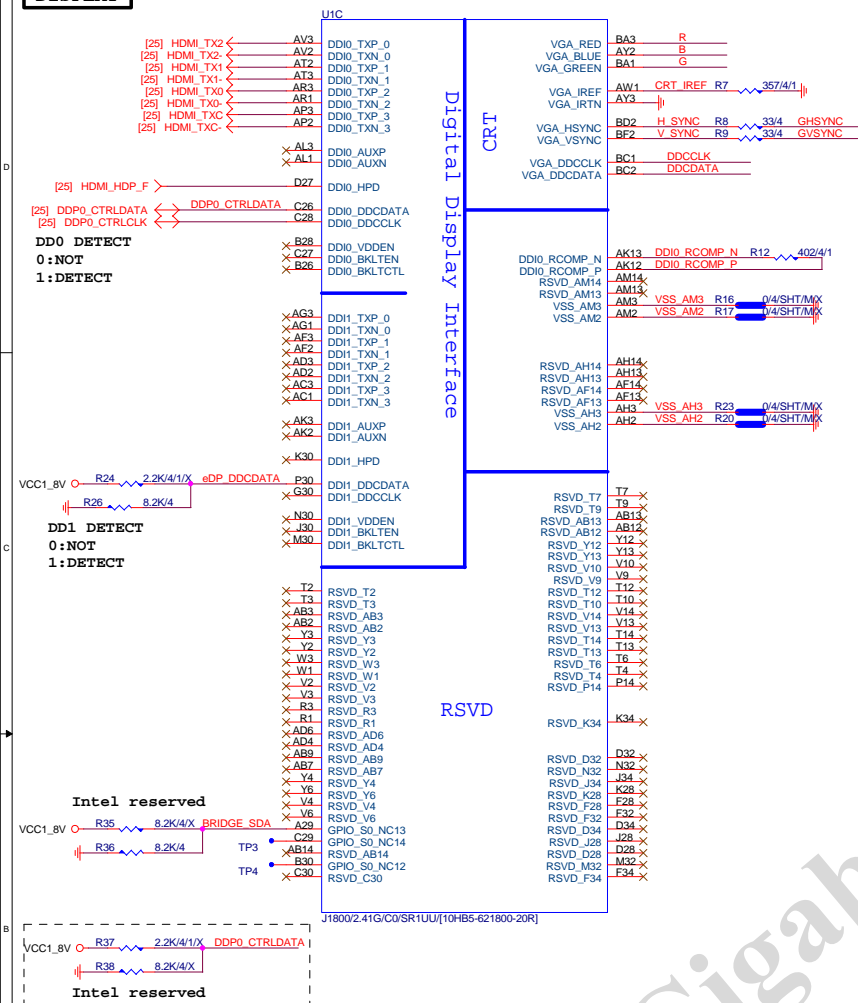
DDR1_35V



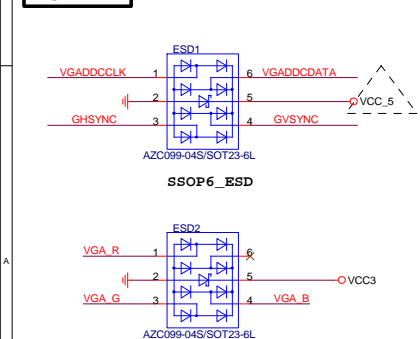
Gigabyte Technology

Title	VLV-M/D MEMROY		
Size B	Document Number	GA-J1800N-D2H	
Date:	Friday, April 18, 2014	Sheet	4 of 26

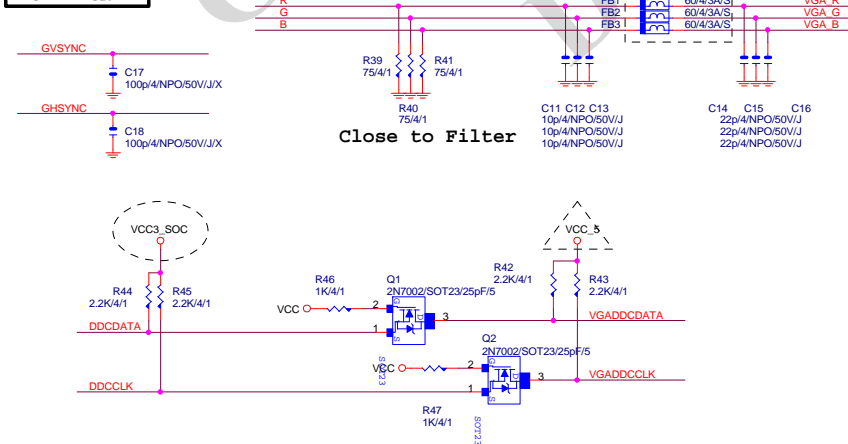
DISPLAY



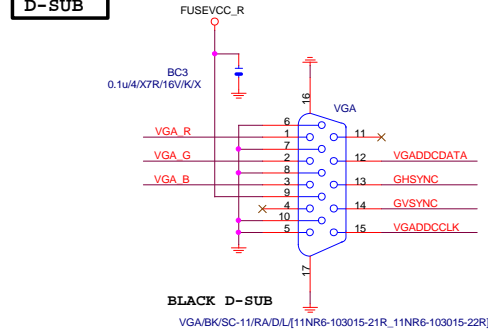
VGA ESD

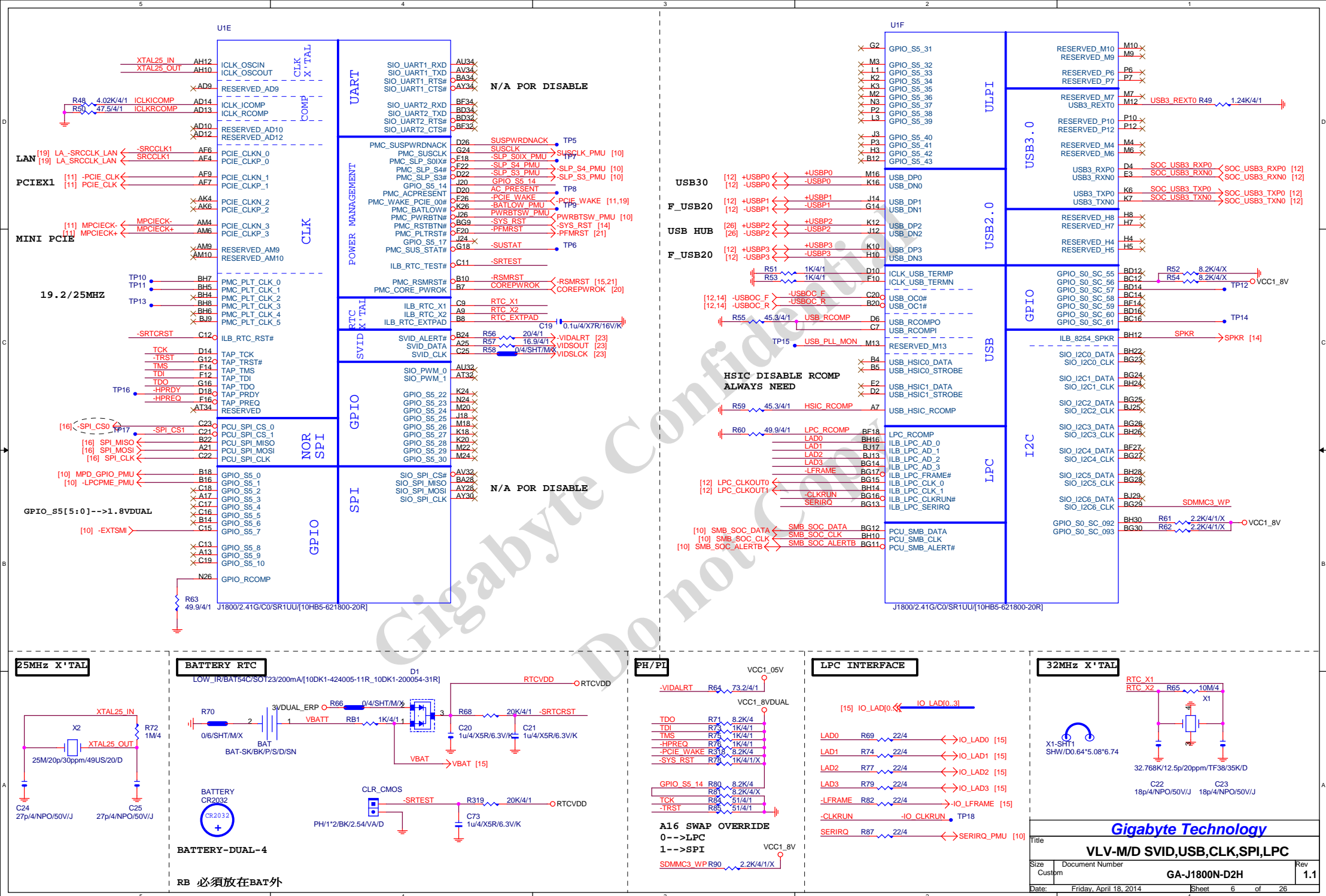


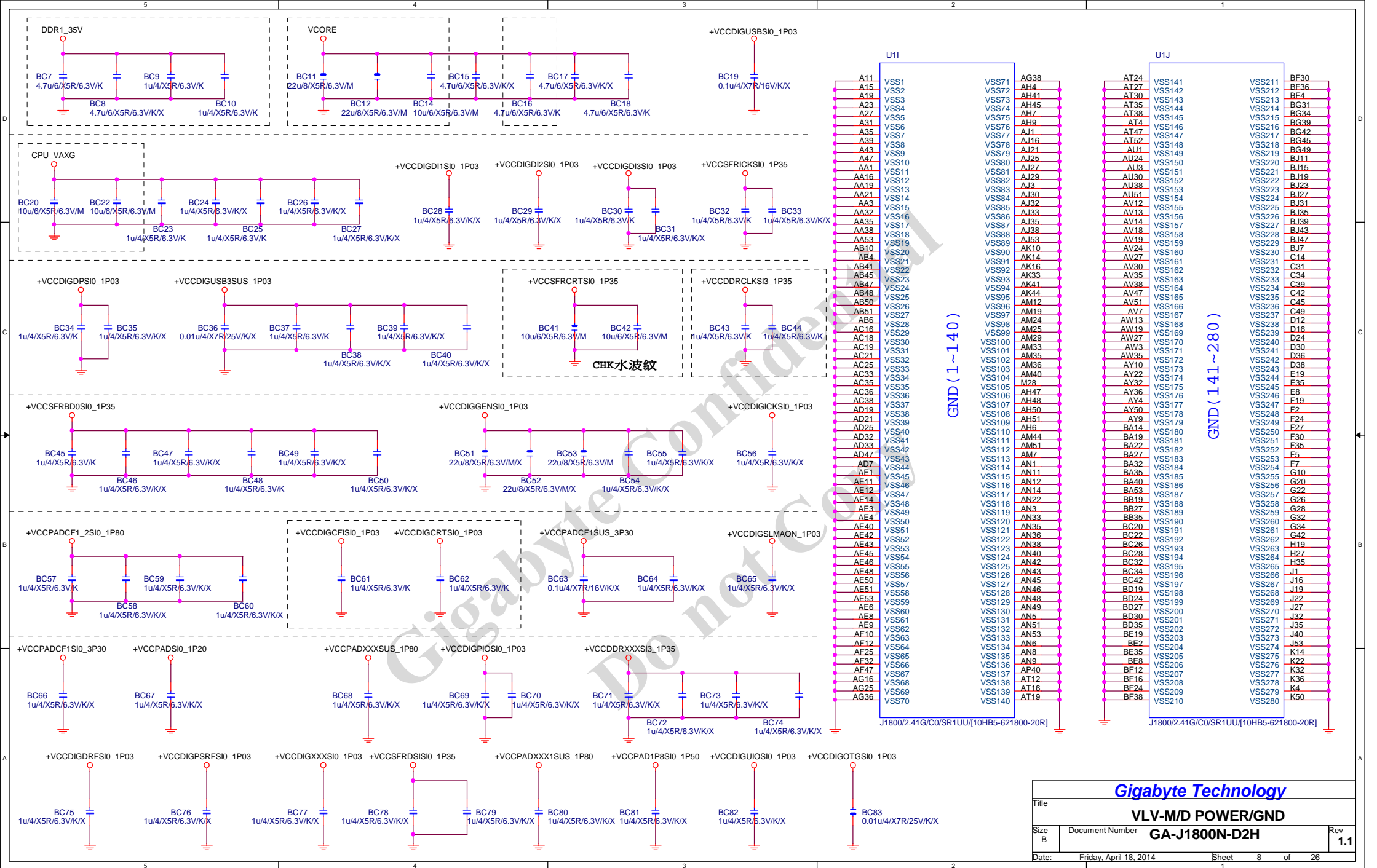
VGA SIGNAL



D. GUP







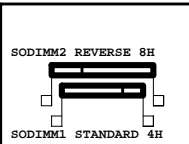
Gigabyte Technology

Title		VLV-M/D POWER/GND	
Size	Document Number	GA-J1800N-D2H	
B			
Date:	Friday, April 18, 2014	Sheet	8 of 26

DUAL CHANNEL

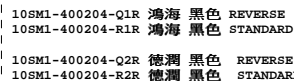


DDR3-SODIMM-STD-4H



DDR3 SDRAM SO-DIMM

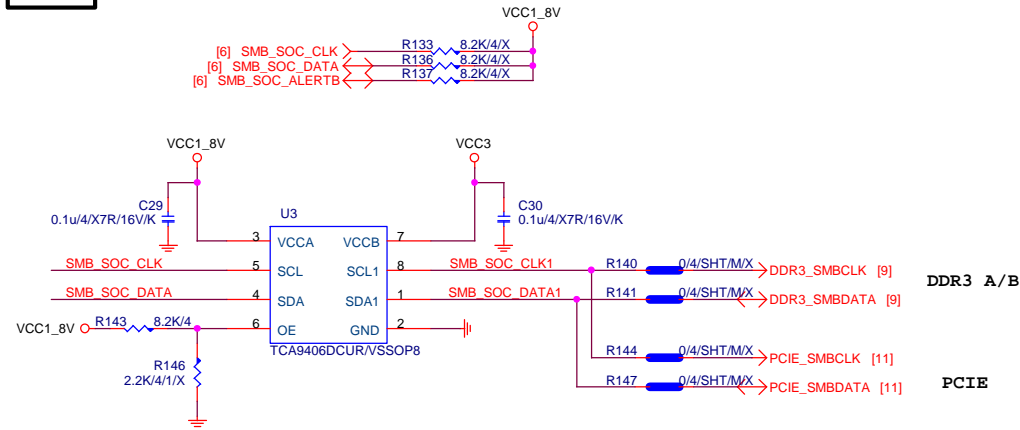
DDR3-SODIMM-RVS-8H



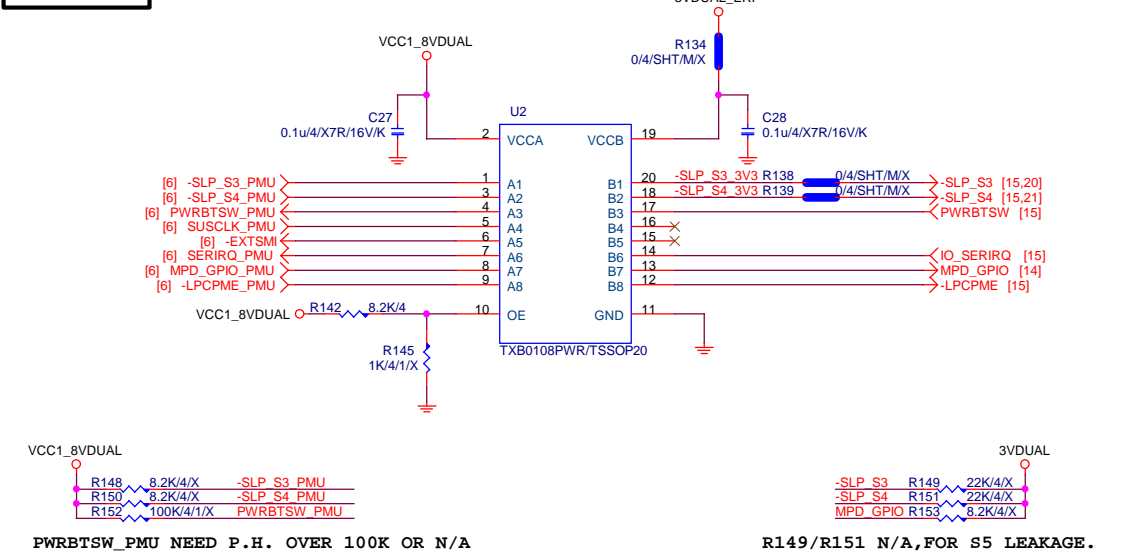
The four diagrams illustrate the connection of the DDR1_35V supply to different DDR pins:

- Top Left:** DDR1_35V is connected to pin R131. A 1K/4/1 resistor (TR5) is connected to the supply, and another 1K/4/1 resistor (TR8) is connected to ground. A decoupling capacitor (BC84, 0.1u/40X7R/16V/K) is connected between the pin and ground. The signal line is labeled VREF_QDDRA.
- Top Right:** DDR1_35V is connected to pin R133. A 1K/4/1 resistor (TR6) is connected to the supply, and another 1K/4/1 resistor (TR7) is connected to ground. The signal line is labeled VREF_DDRA.
- Bottom Left:** DDR1_35V is connected to pin R132. A 1K/4/1 resistor (TR9) is connected to the supply, and another 1K/4/1 resistor (TR11) is connected to ground. A decoupling capacitor (BC85, 0.1u/40X7R/16V/K) is connected between the pin and ground. The signal line is labeled VREF_QDDRB.
- Bottom Right:** DDR1_35V is connected to pin R134. A 1K/4/1 resistor (TR10) is connected to the supply, and another 1K/4/1 resistor (TR12) is connected to ground. The signal line is labeled VREF_DDRB.

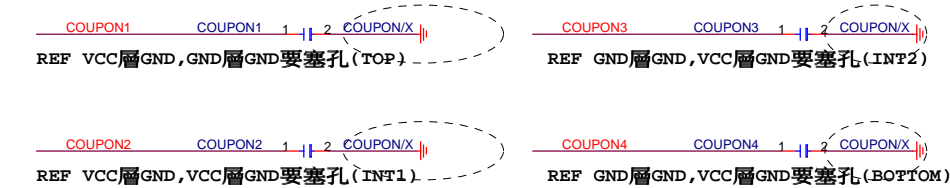
SMBUS



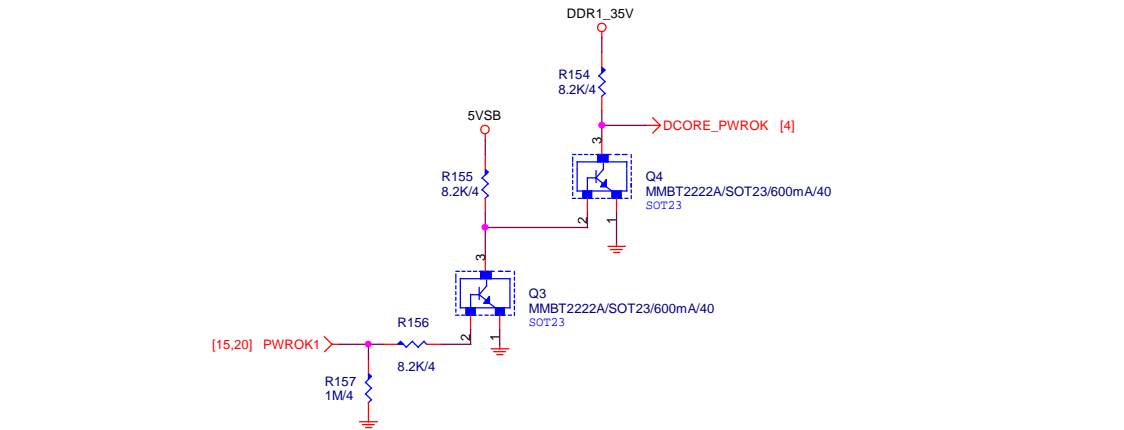
SIGNAL L/S



COUPON



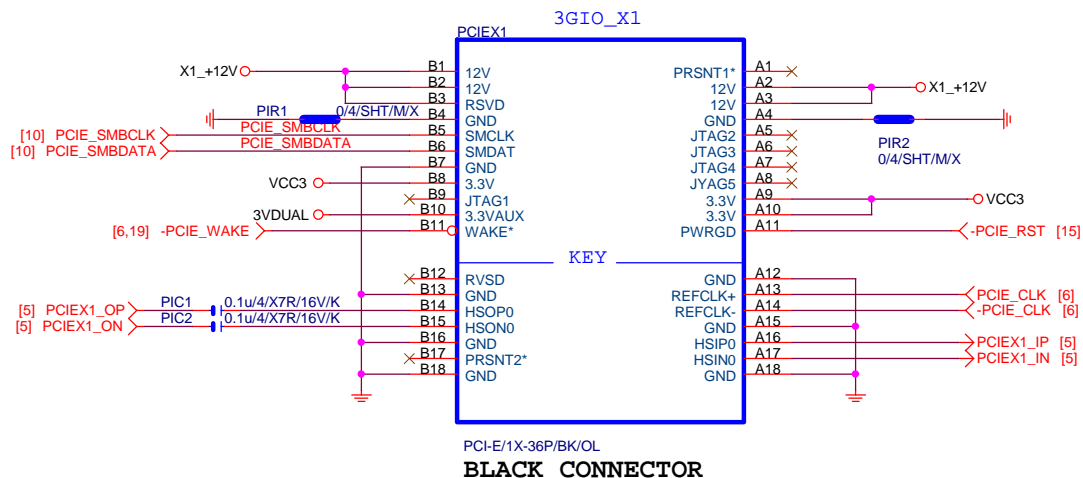
DDR PWROK



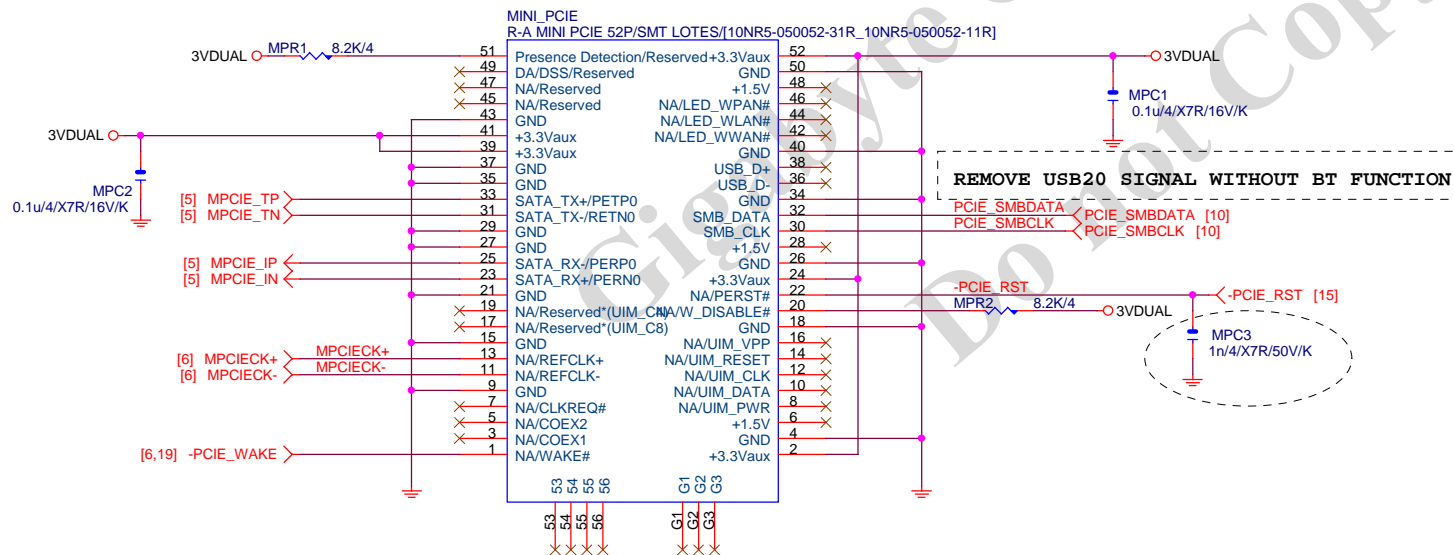
Gigabyte Technology

Title		
SMBUS,SIGNAL L/S		
Size B	Document Number	Rev
	GA-J1800N-D2H	1.1
Date:	Friday, April 18, 2014	Sheet 10 of 26

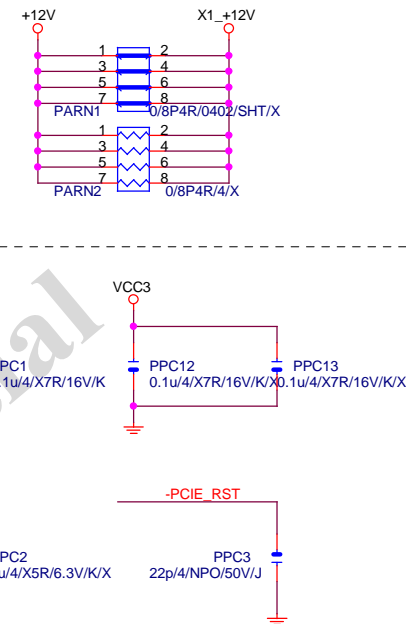
PCIEX1 SLOT



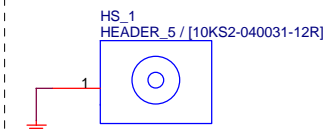
mini PCI-E



MINI_PCIE52P-HALF-A
BLACK CONNECTOR



SMD HEADER:

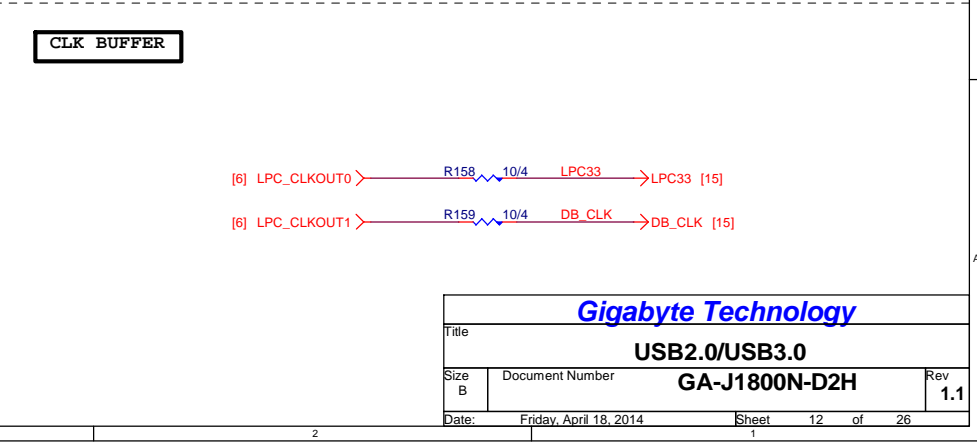
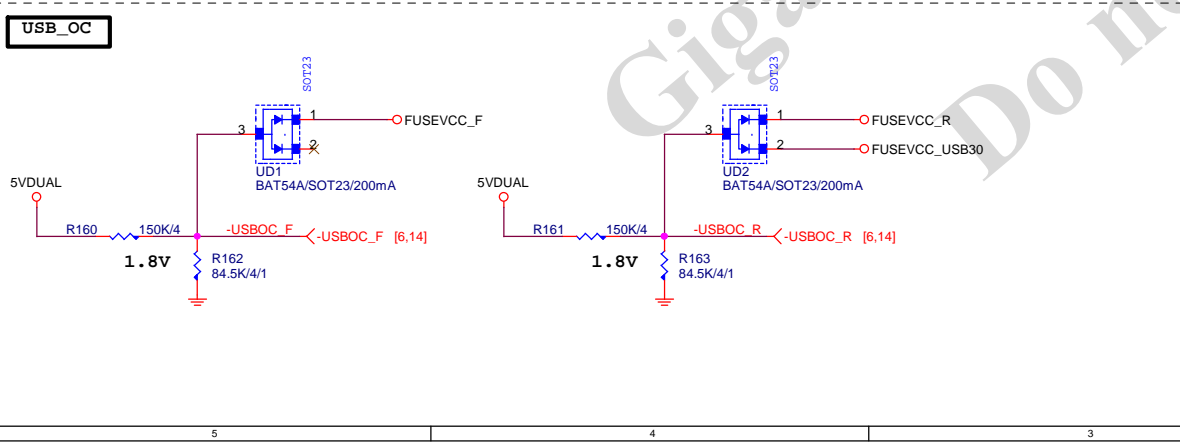
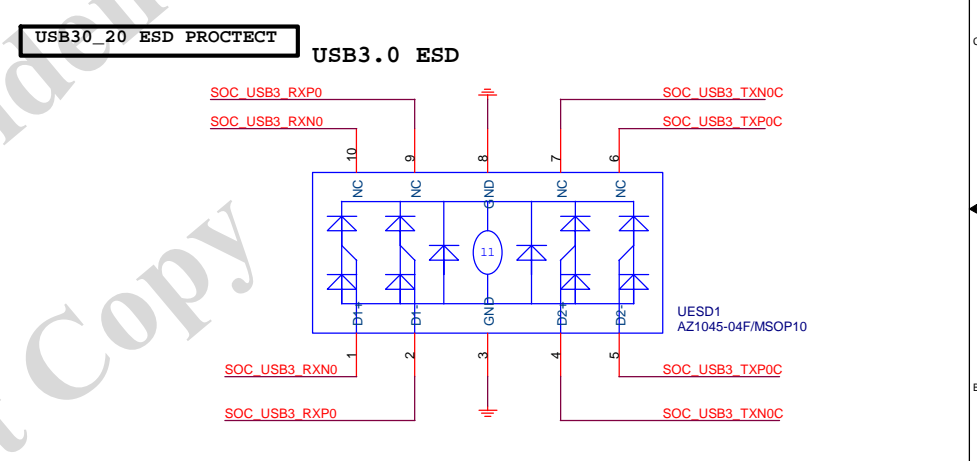
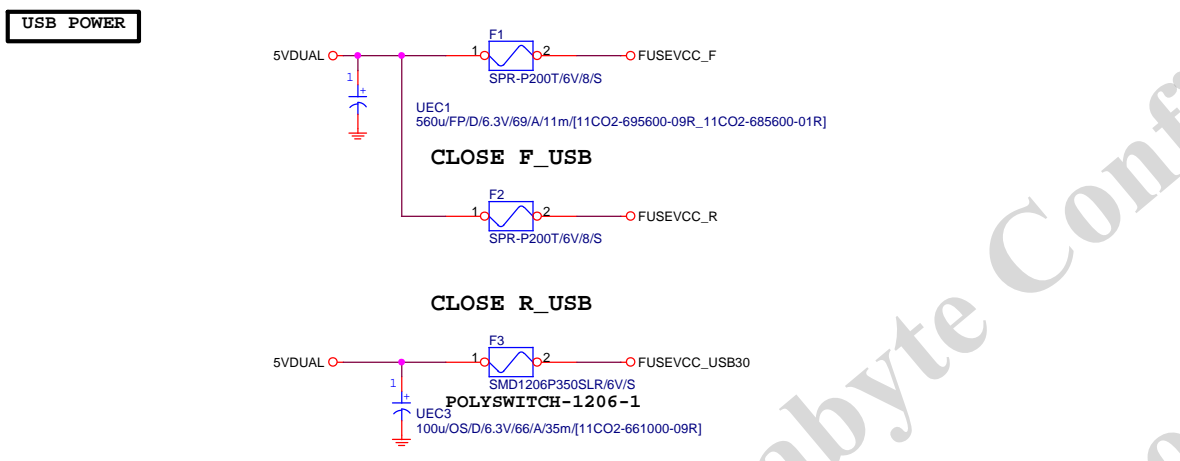
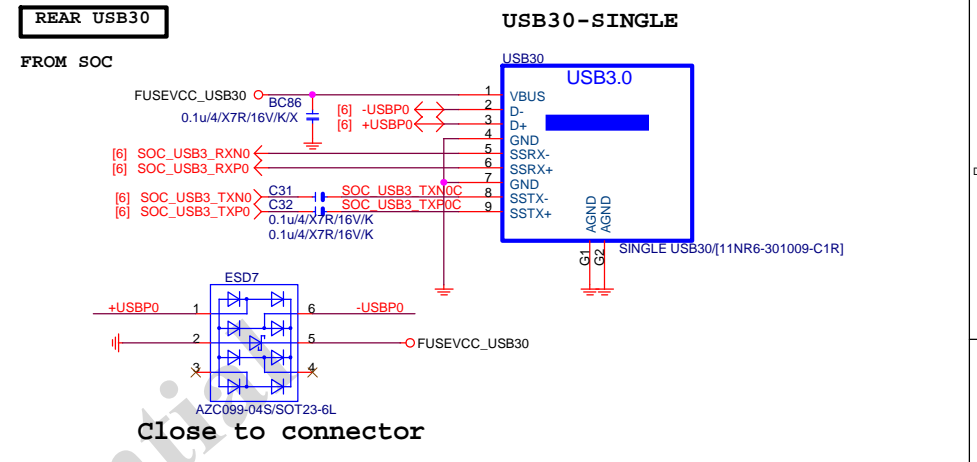
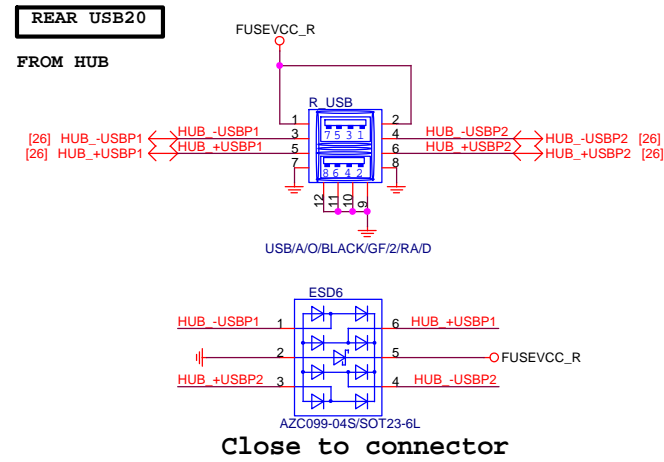
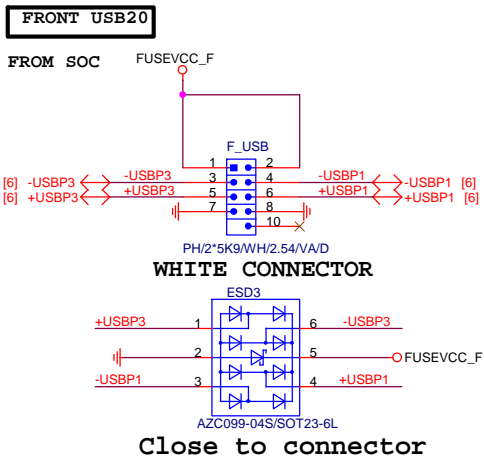


SCREW:

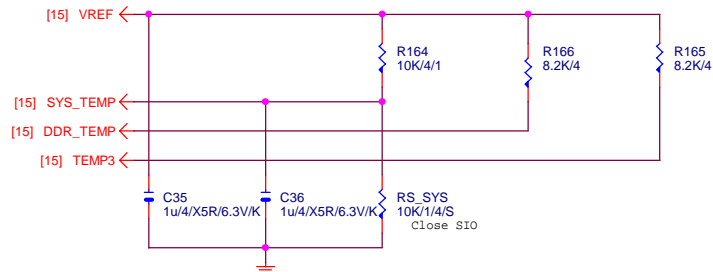


SCREW/[12KS2-010204-31R]

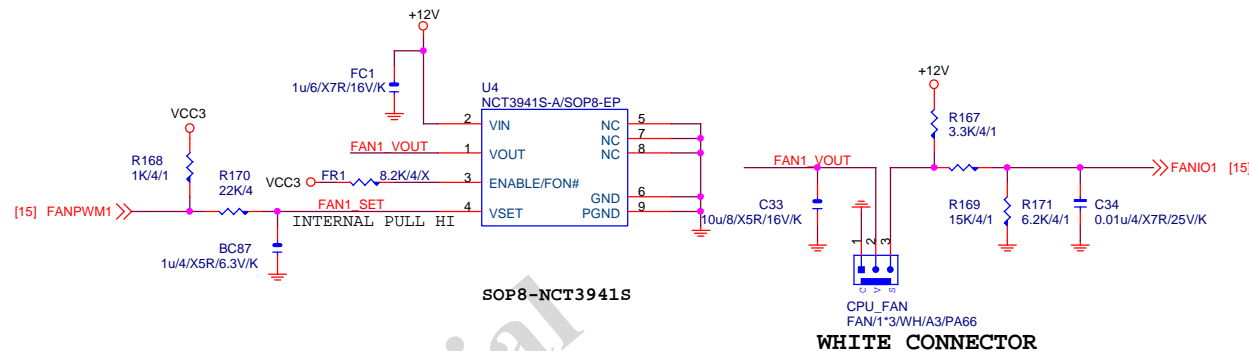
AT THE SAME LOCATION



TEMP H/W MONITOR

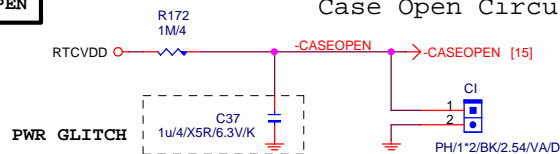


CPU SMART FAN

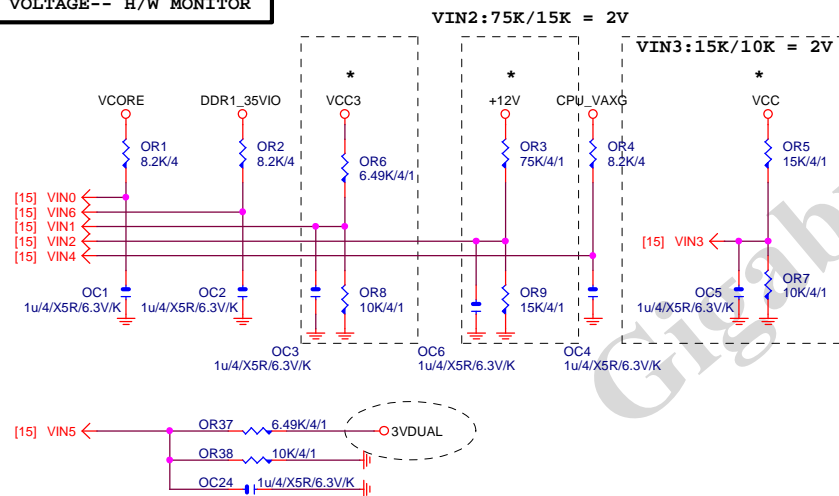


CASE OPEN

Case Open Circuits



VOLTAGE-- H/W MONITOR

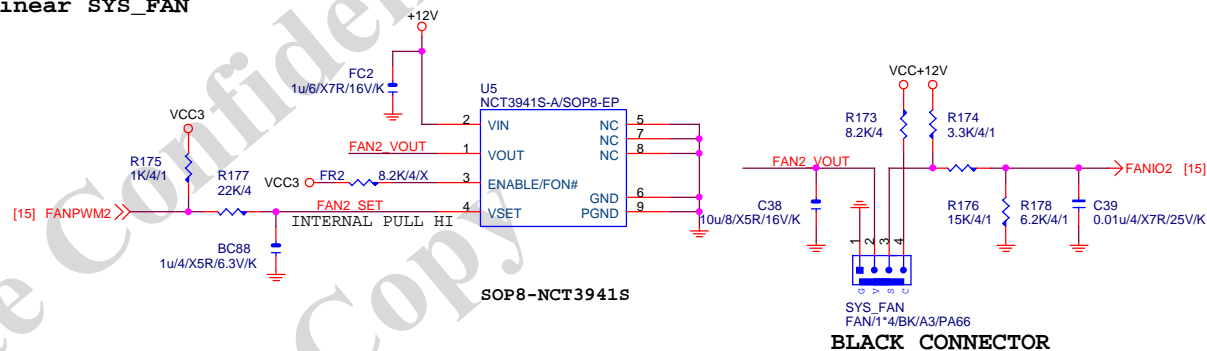


-PROHOT

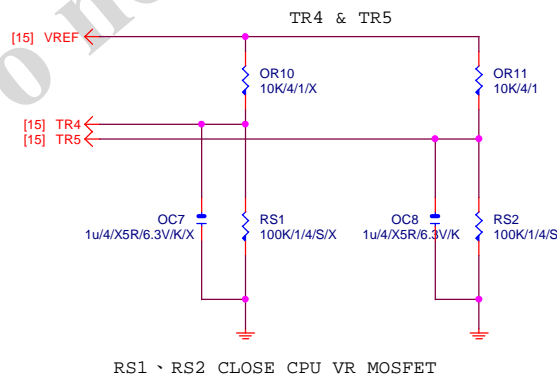
N/A

SYS SMART FAN

Linear SYS_FAN



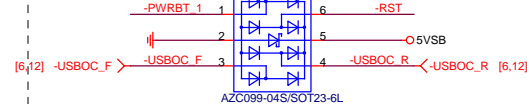
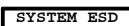
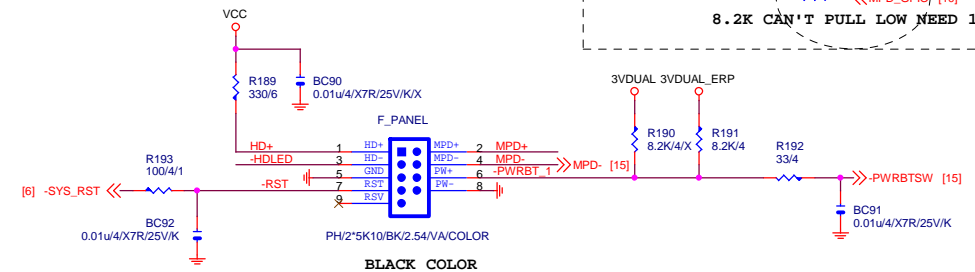
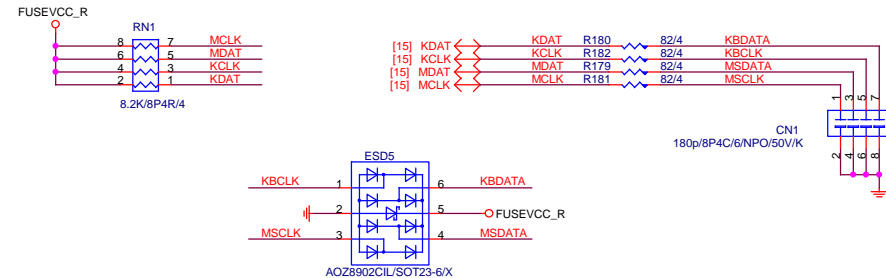
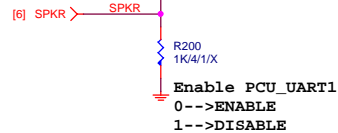
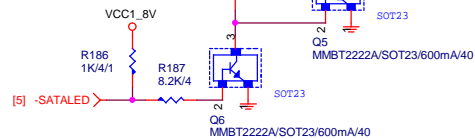
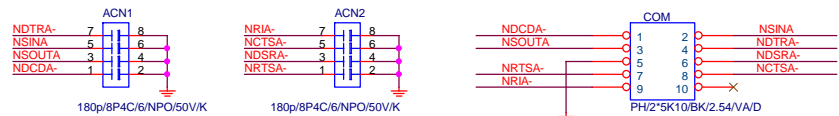
I/O IT8620 THERMAL SENSOR



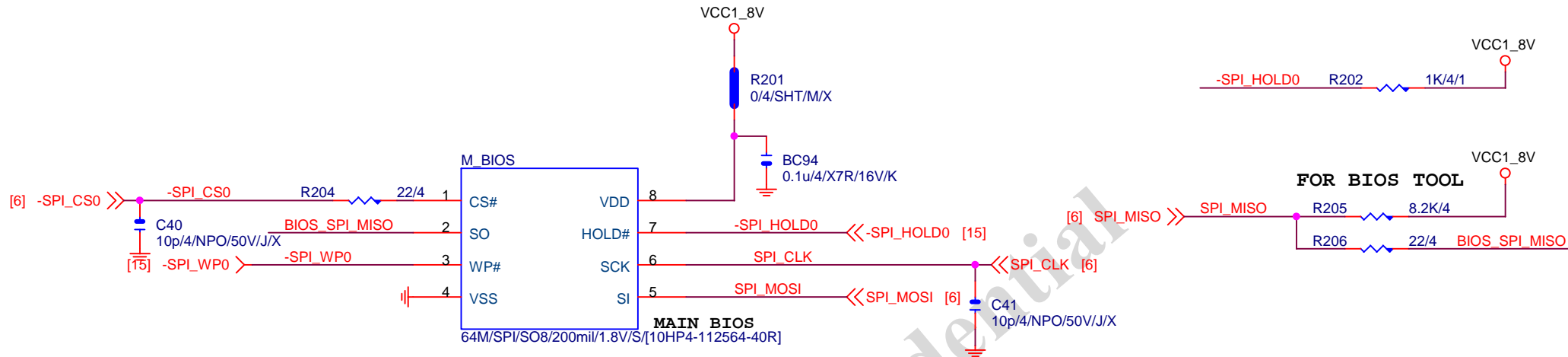
RS1、RS2 CLOSE CPU VR MOSFET

Gigabyte Technology

Title		HWM,FAN CTRL_OV	
Size	Document Number	GA-J1800N-D2H	
Custom		Rev 1.1	
Date:	Friday, April 18, 2014	Sheet	13 of 26



MAIN BIOS



SPI ROM(1.8V)

Gigabyte Technology

Title

SPI BIOS

Size
Custom

Document Number

GA-J1800N-D2H

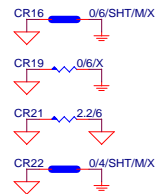
Rev
1.1

Date:

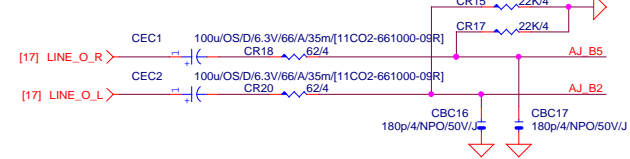
Friday, April 18, 2014

Sheet

16 of 26



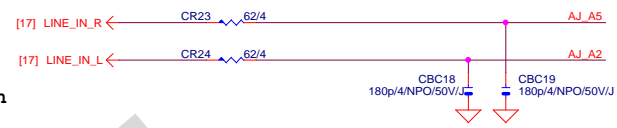
LINE-OUT



LINE-IN

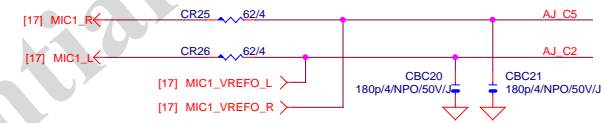
Verify MIC function
in LINE-in

Only reserved for ALC888

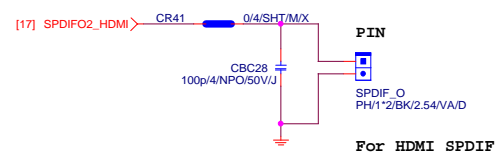


For 889A/888

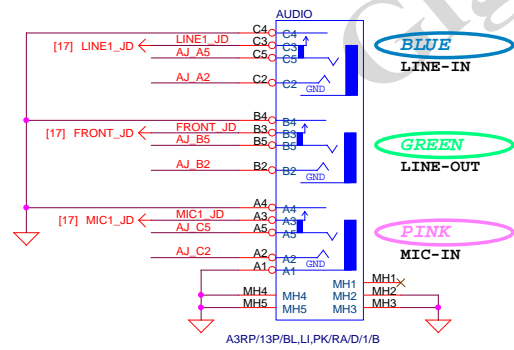
MIC-IN



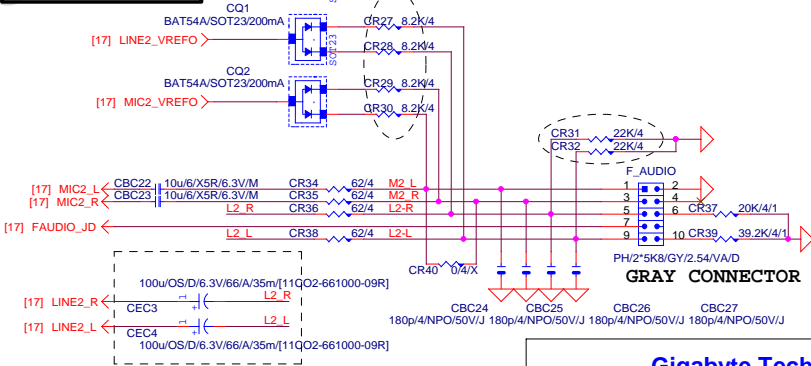
SPDIF_OUT



For HDMI SPDIF



AZALIA FRONT PANEL



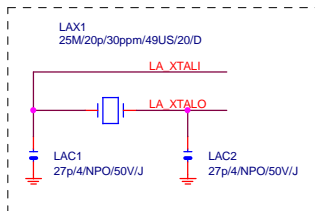
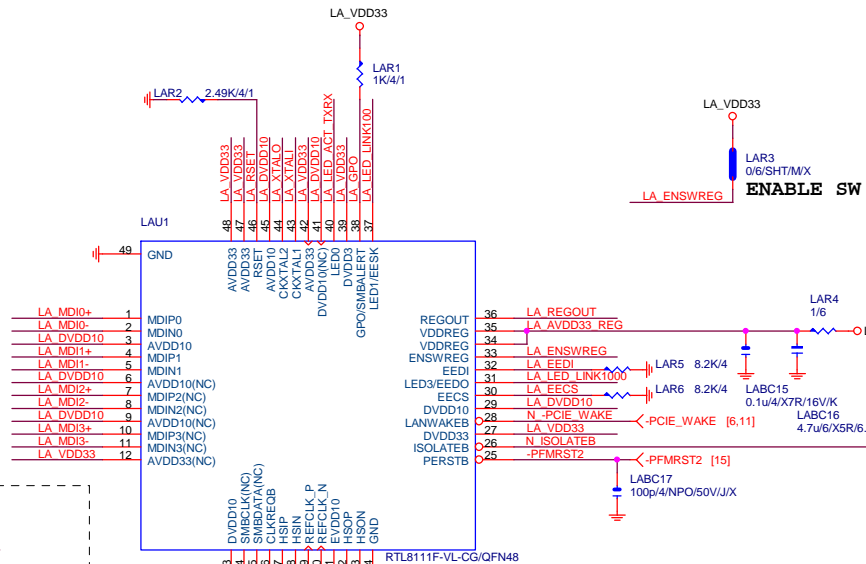
Gigabyte Technology

AUDIO JACK

GA-J1800N-D2H

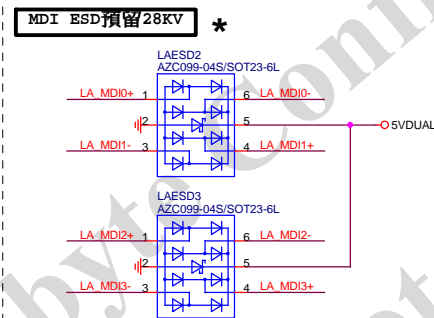
Rev 1.1

LAN RTL8111F-VL

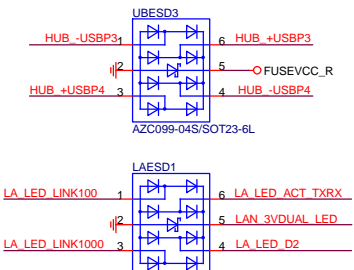


LA_ ML-->80歐姆:[15/5/5/5/15]

SRCCLK-->50歐姆:[18/4/10/4/18]



LAN CONNECTOR ESD



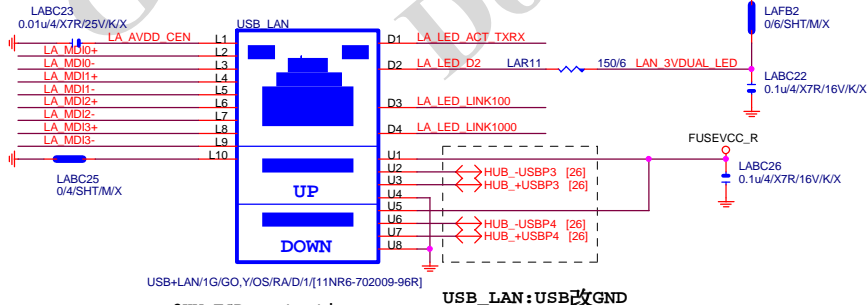
使用RU9 USB_LAN可省略LAESD1保護LED

EMI SHORT PAD



PS:視EMI需求

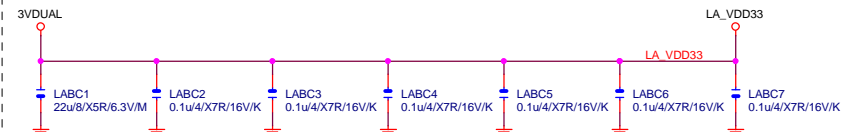
LA MDI-->100歐姆:[20/4/8/4/20]



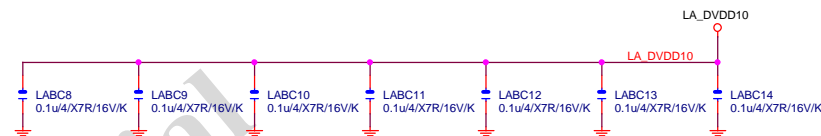
9KV ESD protection

USB LAN:USB~~2~~GND

LAN POWER

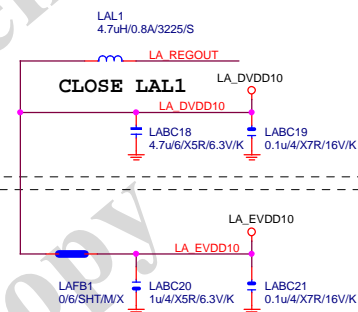


(CLOSE LAU1 PIN:12,27,39,42,47,48)



(CLOSE LAU1 PIN3,6,9,13,29,41,45)

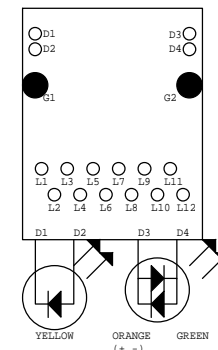
(CLOSE LAU1 PIN36)



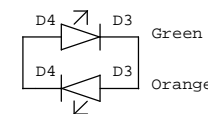
(CLOSE LAU1 PIN21)

Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

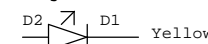


Dual Color LED



Green

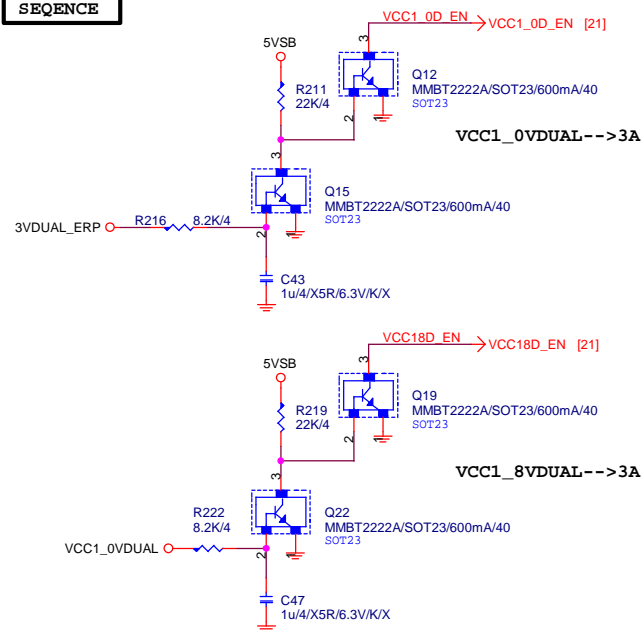
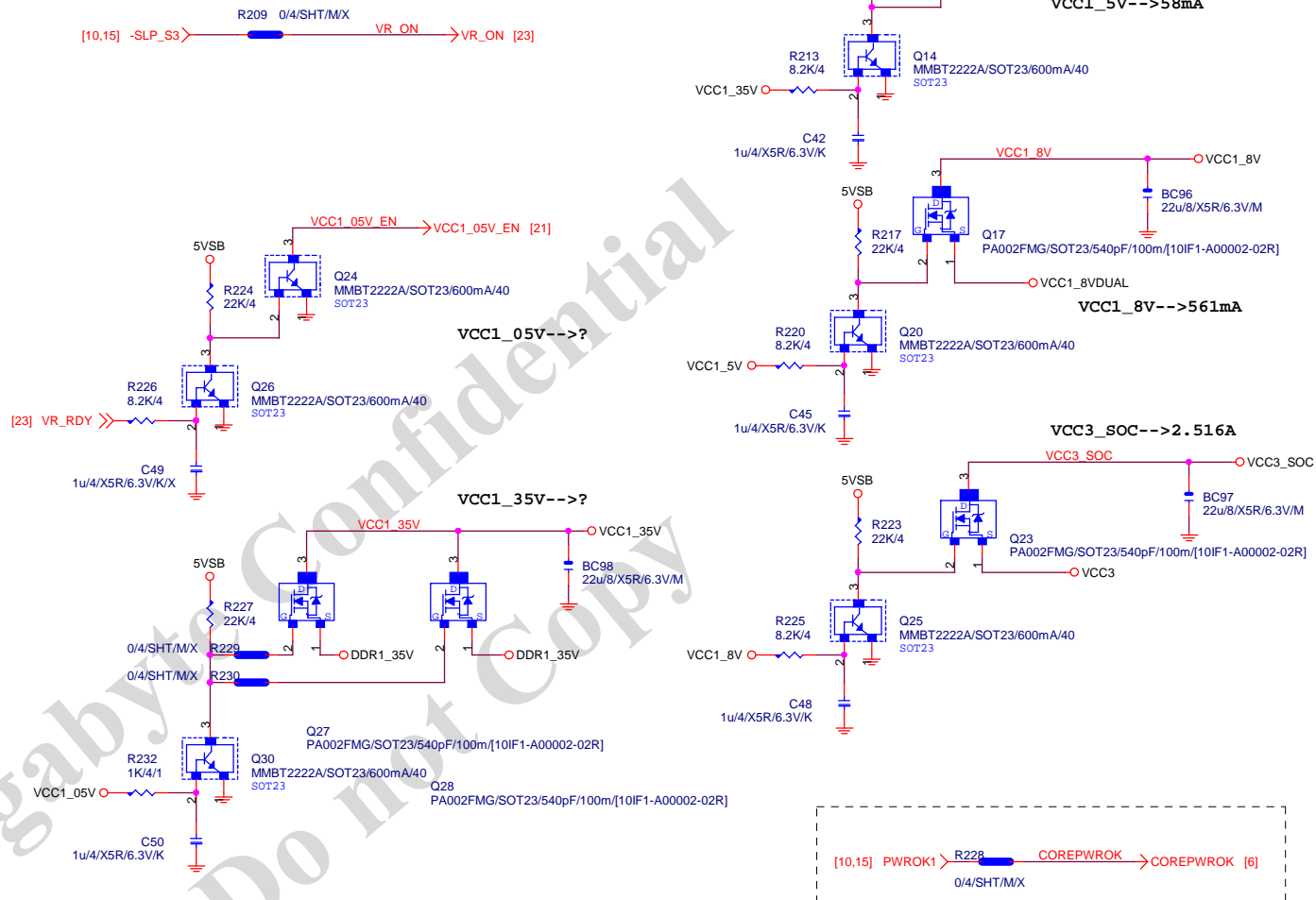
Single Color LED



- Yellow

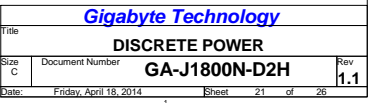
Gigabyte Technology

Title				RTL111F-VL			
Size	Custom	Document Number				Rev	1.1
		GA-J1800N-D2H					
Date:	Friday, April 18, 2014			Sheet	19	of	26

STANDBY
SEQUENCEMAIN
SEQUENCE

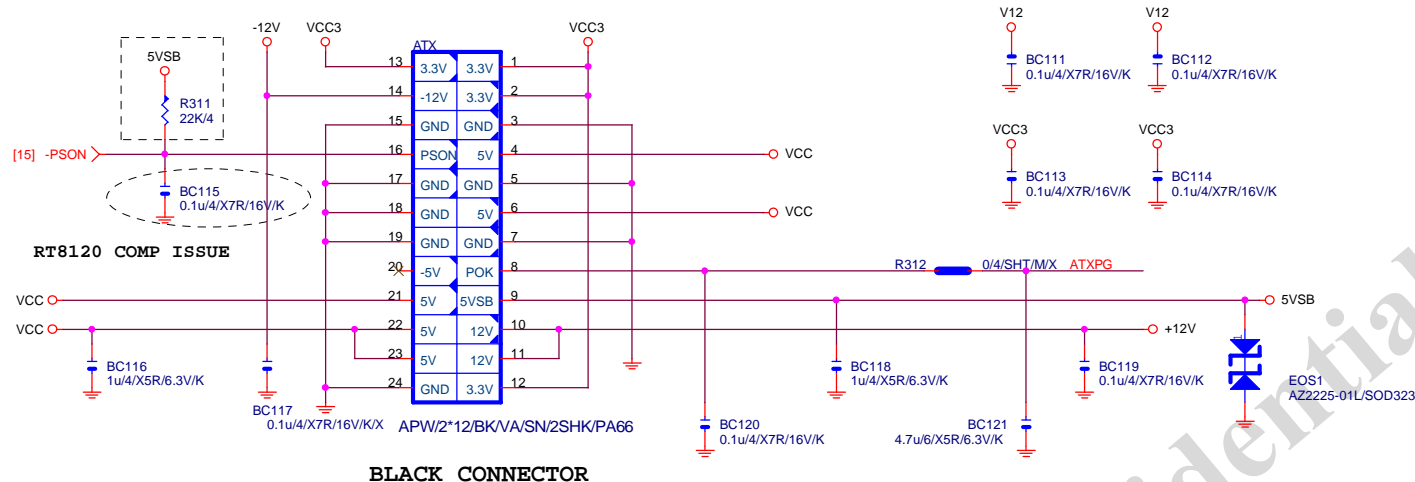
Gigabyte Technology

Title			POWER SEQUENCE	
Size B	Document Number	GA-J1800N-D2H		Rev 1.1
Date:	Friday, April 18, 2014	Sheet	20	of 26

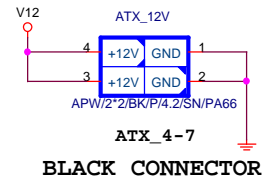


ATXX24 POWER CONNECTOR

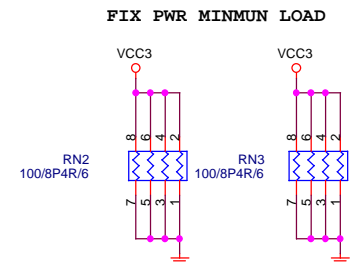
【技術通報R&D技術通報155】



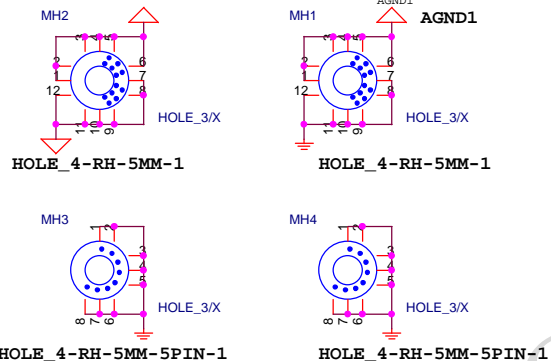
ATXX4 POWER CONNECTOR



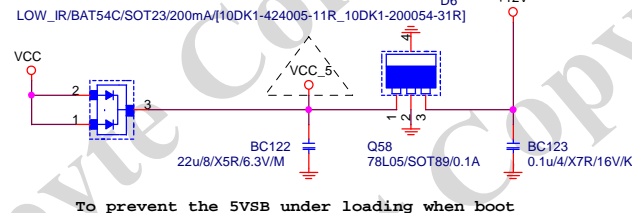
MIN. LOAD



MB LOCATION

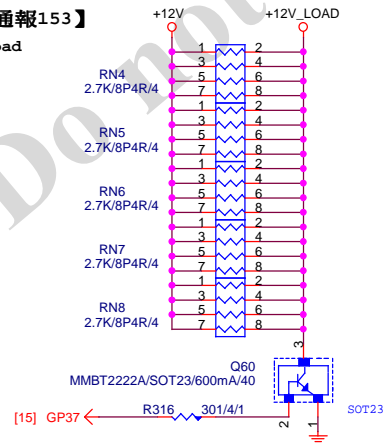


FIX POWER SUPPLY MIN LOAD +5V ISSUE

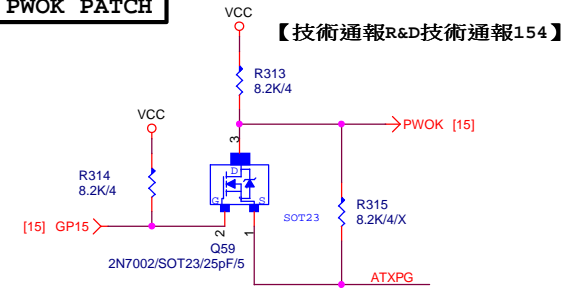


【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



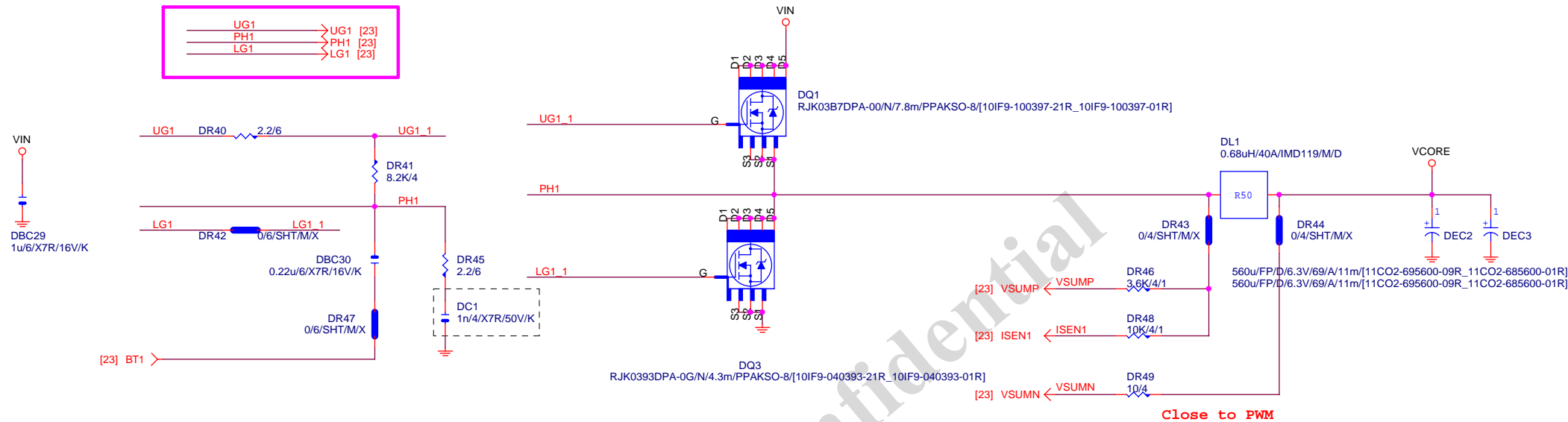
PWOK PATCH



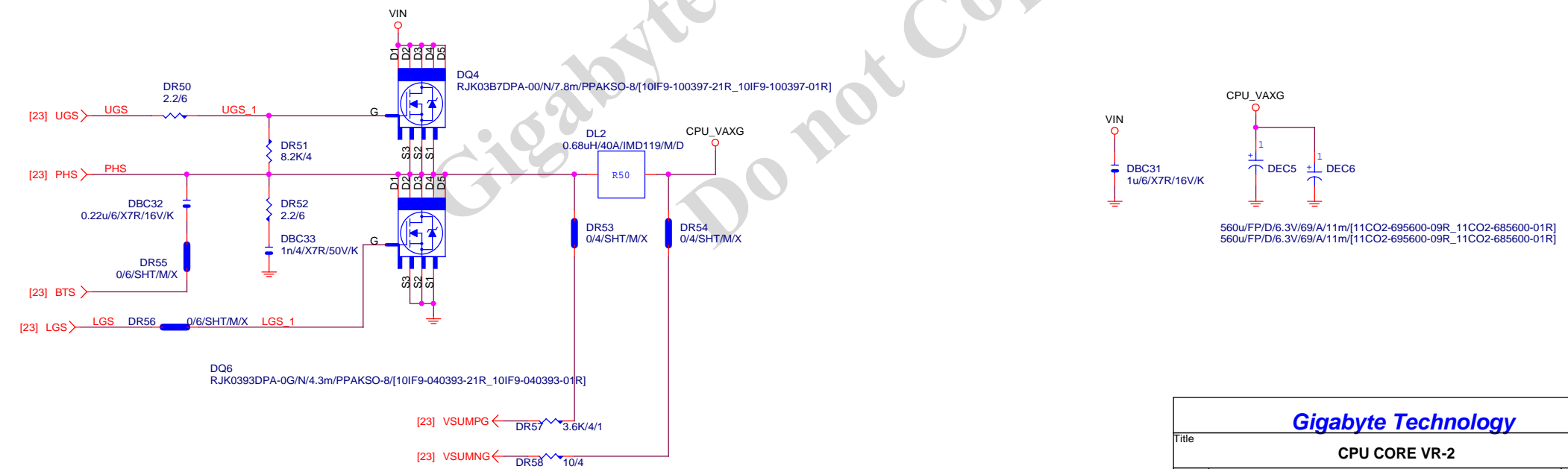
Gigabyte Technology

Title		
ATX CONNECTOR		
Size B	Document Number	Rev
	GA-J1800N-D2H	1.1
Date:	Friday, April 18, 2014	Sheet 22 of 26

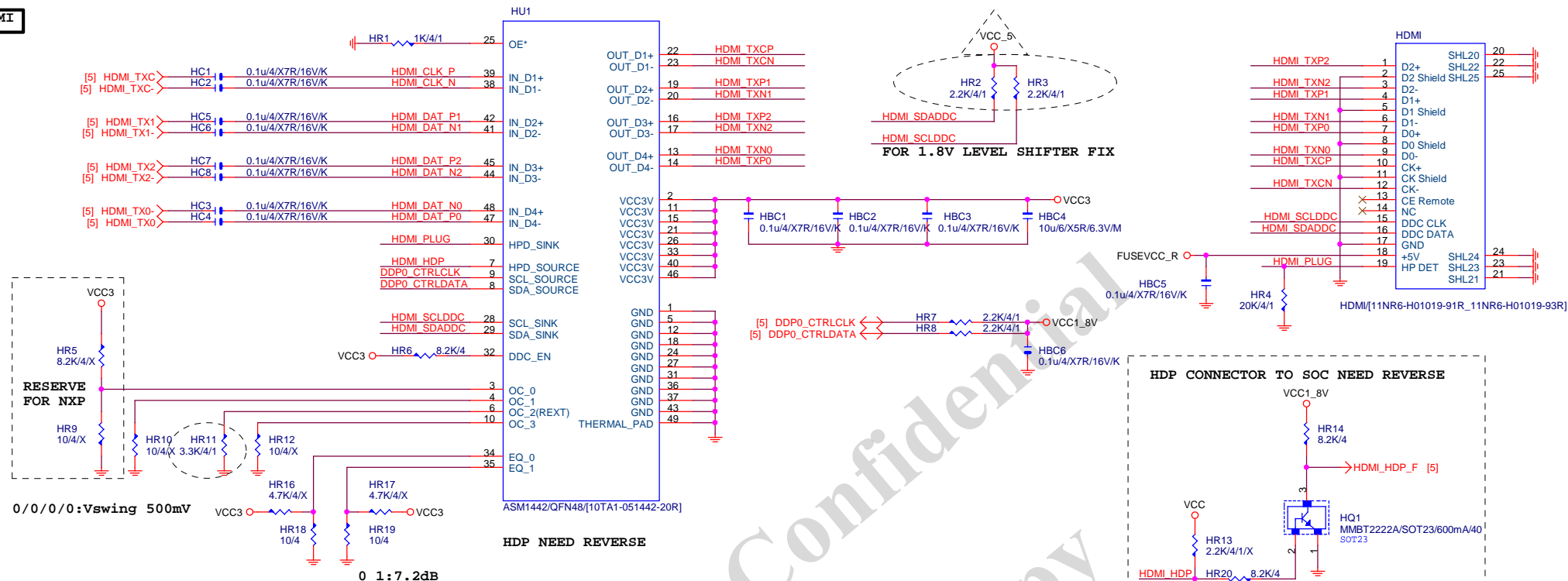
VCORE



VAXG

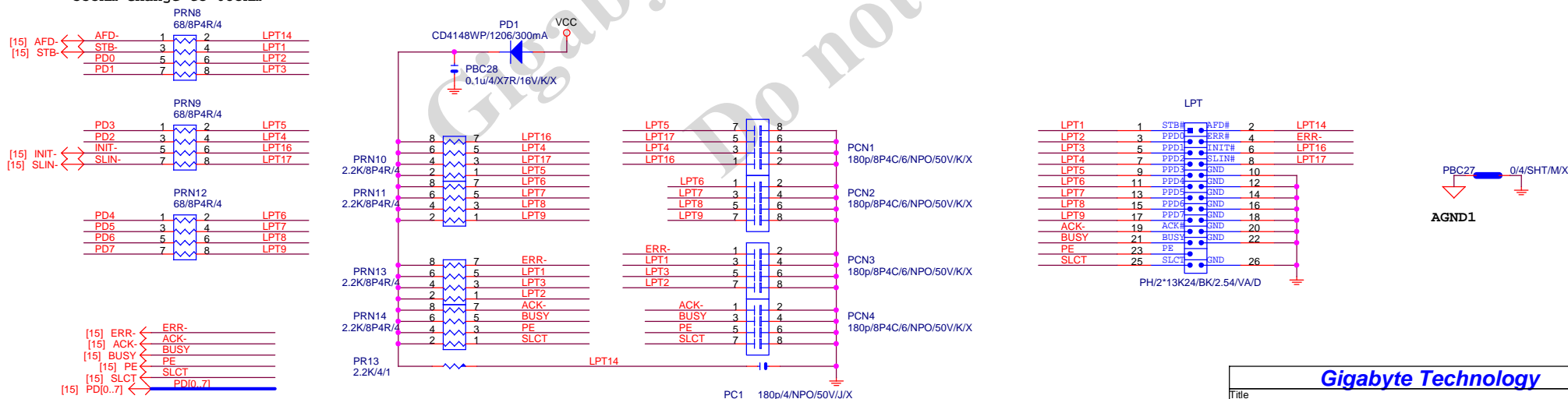


Gigabyte Technology			
Title			
CPU CORE VR-2			
Size	Document Number	GA-J1800N-D2H	
Custom		Rev 1.1	
Date:	Friday, April 18, 2014	Sheet	24 of 26

HDMI

LPT PORT

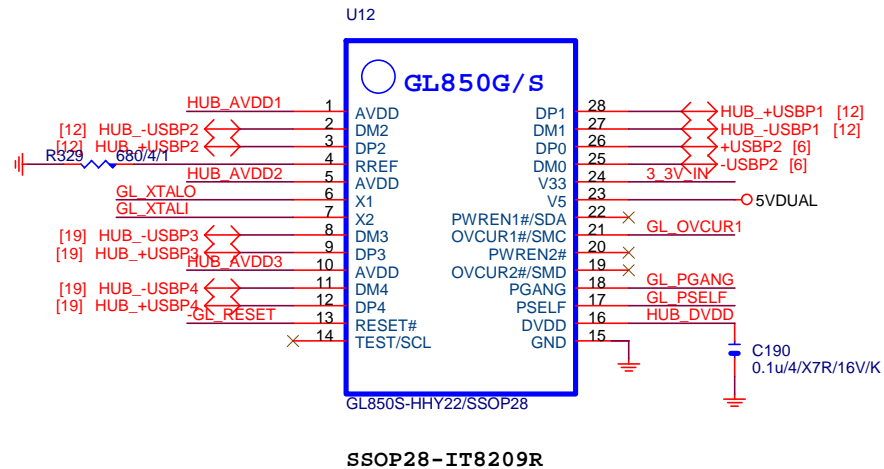
【技術通報R&D技術通報151】
33ohm Change to 68ohm



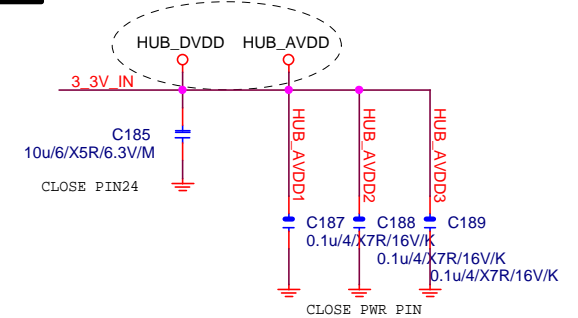
Gigabyte Technology

Title			
HDMI,LPT			
Size	Document Number		Rev
Custom	GA-J1800N-D2H		1.1
Date:	Friday, April 18, 2014	Sheet	25 of 26

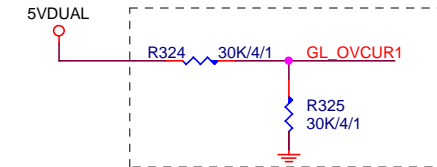
USB20 HUB



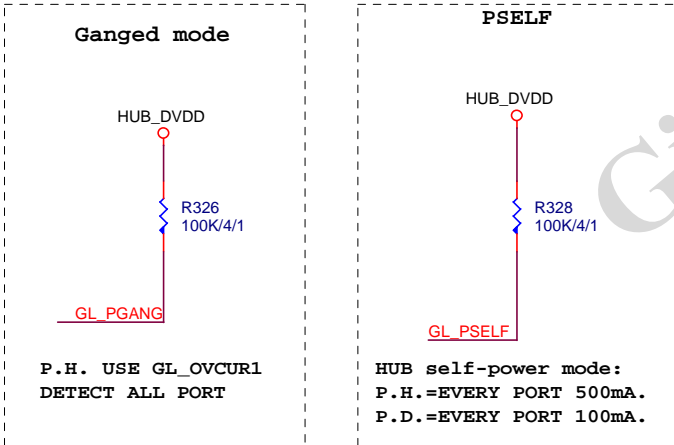
HUB PWR



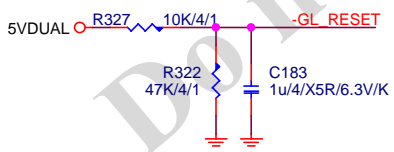
HUB OVER CURRENT SENSE



HUB MODE

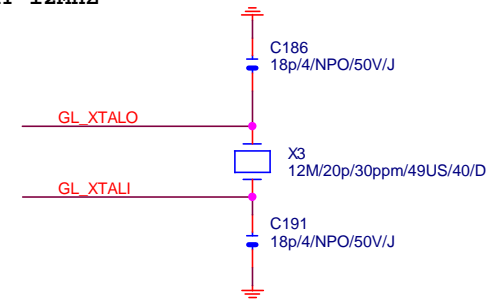


HUB RESET



HUB CRYSTAL

ONLY SUPPORT 12MHZ



Gigabyte Technology			
Title			
HUB GL850GS			
Size	Document Number	Rev	
Custom	GA-J1800N-D2H	1.1	
Date:	Friday, April 18, 2014	Sheet	26 of 26